Serial Communication PC to Nexys

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Laboratory exercise number:

Lab. 10

Laboratory exercise name:

Assignment 10

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| Names: | Roll Number | Date |
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Lab description:

The purpose of this laboratory is to learn how program a serial communication between PC and Nexys communication. In previous classes we learnt how to make a link between Nexys to PC via serial communication protocol and this laboratory is to make the same logic but now Nexys is the client.

The material used was:

Nexys 3 by Digilent for the FPGA

ISE Project Naviator for the VHDL compiler and editor

Adept by Digilent for the deployment to the FPGA

Schematics, block diagrams and/or timing diagrams:

Using a frequency divider we obtain the same data at almost the same time than the host. First we wait until data is sent and if a rising edge is detected and there is a change registered on the data obtained by the usb port the register shift their data and store it on a 20bit. The read starts on the start bit when its detected and ends on the end bit. The order and code are the following (frequency divider and 7seg display is from previous labs.):

Record serial

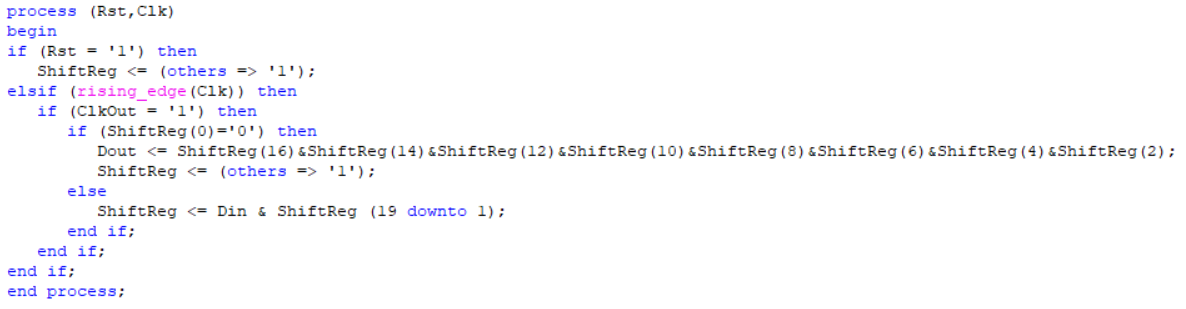
Start bit

Clk

Frequency divider

End bit

Image 1.1



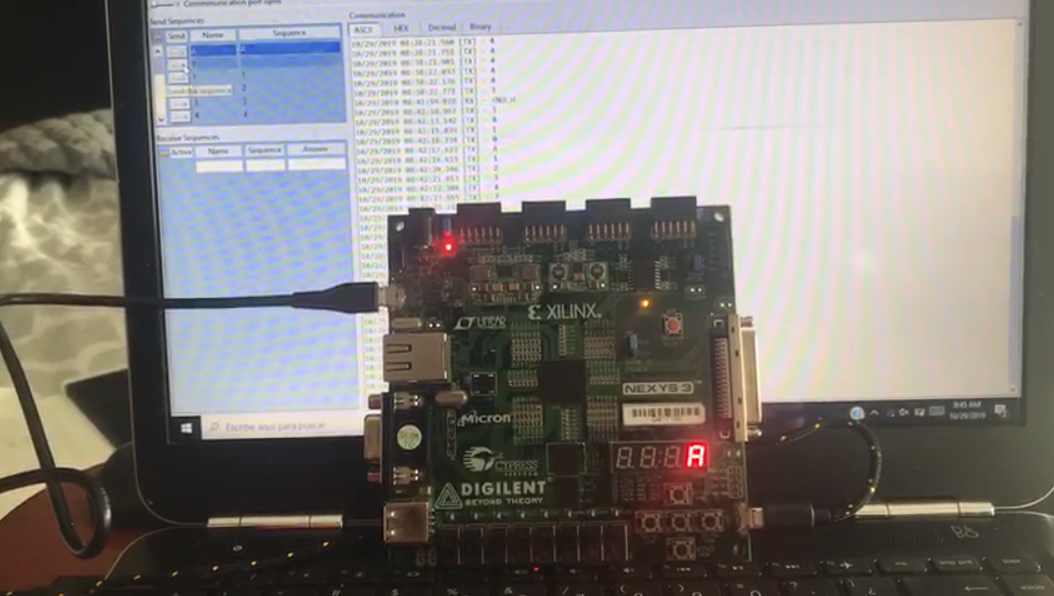
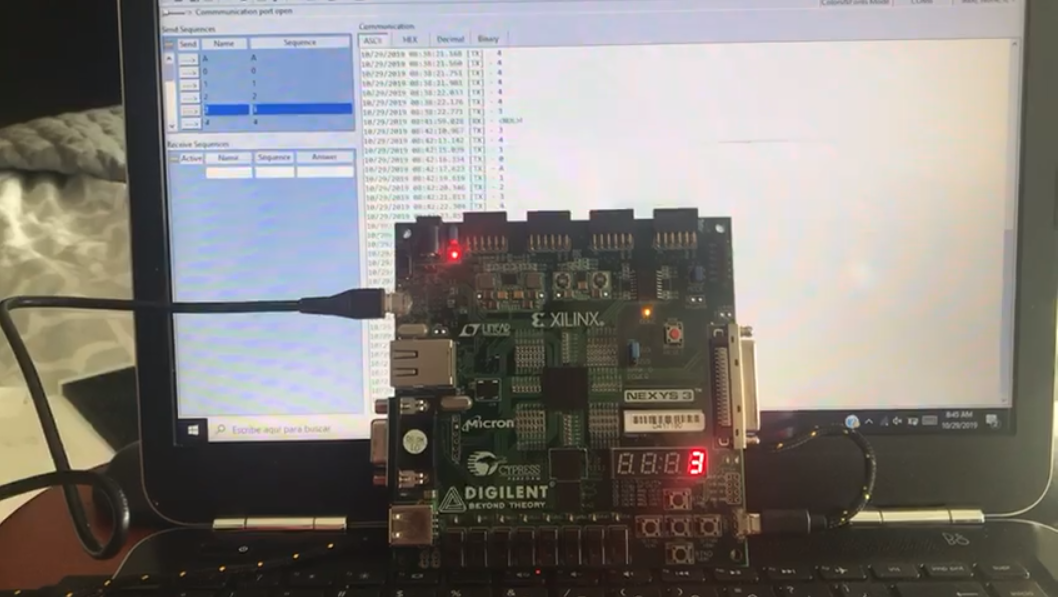
Results obtained:

The result was a successful serial communication from PC to Nexys storing ASCII code when data is received and displayed on the 7-segment display.

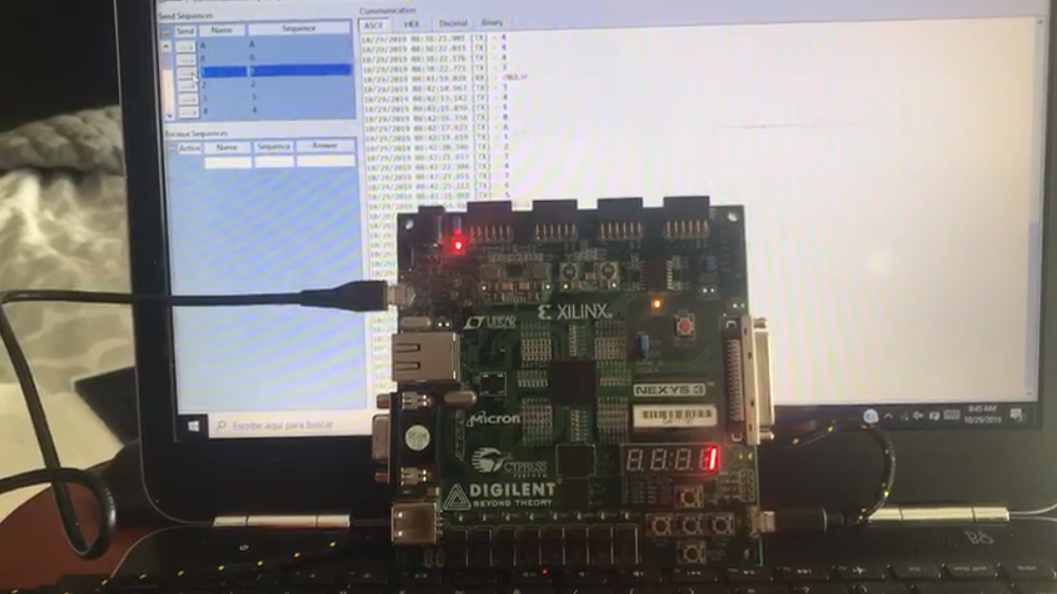
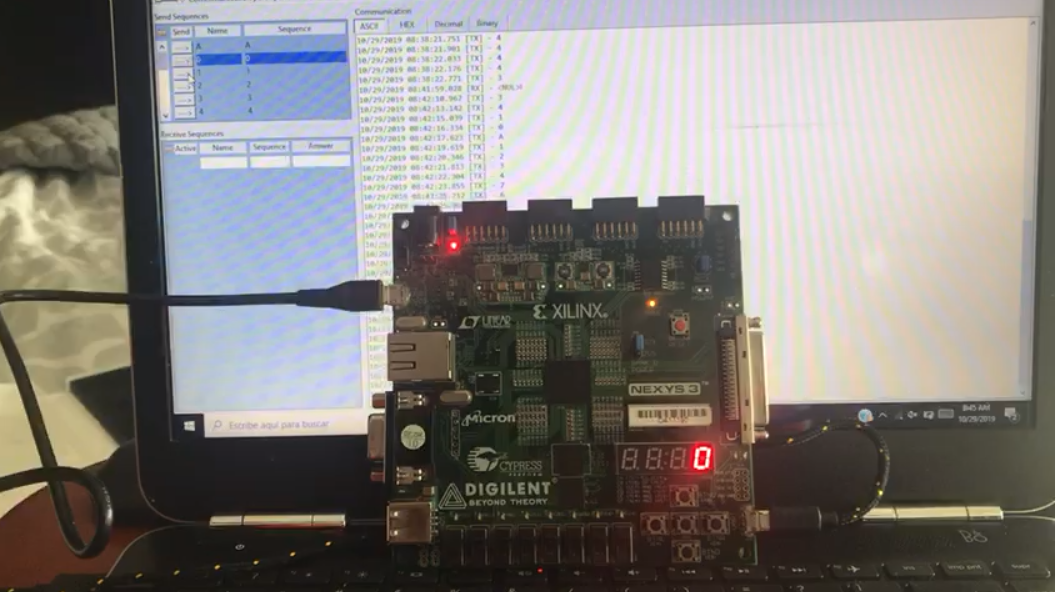
Evidence:

Video: https://youtu.be/uxfayM5hiZQ

Case 1: Case 2:



Case 3: Case 4:



Conclusions:

The serial communication is an easy way to send information via one channel and there is used everywhere because its complicity and versatility.

Problems encountered:

The bits sometimes where not right so to solve this problem we used the way Rick told us, storing two times the bits and we didn’t know what bits must be stored.